IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Chi-An Kao et al.**

Examiner: **Khiem D. Nguyen**

Serial No.: **10/661,793**

Group Art Unit: **2823**

Filed: **09/12/2003**

Confirmation No.: **8353**

For: **CONSTANT AND REDUCIBLE HOLE BOTTOM CD IN VARIABLE POST-CMP THICKNESS AND AFTER-DEVELOPMENT-INSPECTION CD**

CERTIFICATE OF MAILING/FACSIMILE TRANSMISSION PURSUANT TO 37 C.F.R. §1.8

I hereby certify that this correspondence (and anything referred to as being transmitted herewith) is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

Date: _____

Examiner Khiem D. Nguyen
Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF – 37 CFR § 41.41

Commissioner:

This Reply Brief filed pursuant to 37 CFR § 41.41 is timely filed responsive to the Examiner's Answer mailed August 6, 2009. This Reply Brief is filed further to Appellants' Amended Appeal Brief filed April 28, 2009.

The Assistant Commissioner for Patents is hereby authorized to charge any fees necessary to give effect to this filing and to credit any excess payment that may be associated with this communication, to Deposit Account 04-1679.

Respectfully submitted,

Dated: October 5, 2009

/Steve E. Koffs/
Steven E. Koffs, Reg. No. 37,163
Attorney for Appellants

DUANE MORRIS LLP
30 S. 17th St.
Philadelphia, PA 19103-4196
Telephone: (215) 979-1250
Facsimile: (215) 689-2744

Supplemental Arguments Responsive to Examiner's Answer

In the Examiner's Answer ("ANSWER") mailed August 6, 2009, the Examiner reiterates the rejection of claims 8-11 and 15-17 under 35 U.S.C. § 102(e) as being anticipated by Sahin, et al. (U.S. Patent Publication 2003/0220708), hereinafter "Sahin." The ANSWER relies heavily upon the disclosure that appears in FIG. 8A(1) of Sahin and related parts of the specification, to support the rejections. Appellants respectfully submit that FIG. 8A(1) and the corresponding portions of the specification clearly show that Sahin does not enablingly teach the feature of assuring that CD's (critical dimensions) are within design specification limits by communicating with the means for creating an opening through a layer of etch resist material, i.e., (collectively) the lithography tools to **control** the critical dimensions.

In order to maintain a rejection under 35 U.S.C. § 102, each claim element must be found in the anticipating reference used by the Examiner. MPEP Section 2131 states: TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Moreover, in Forest Laboratories, Inc. v. Ivax Pharmaceuticals, Inc., 501 F.3d 1263, 84 USPQ2d 1099 (Fed. Cir. 2007), the Federal Circuit held that a prior art reference must be enabling to support an anticipation rejection.

The claims under appeal include independent claims 8, 15 and 16. Independent claim 8 recites that the feedback mechanism assures that the CD is within specification by communicating with the lithography tool to control the CD by **implementing corrections** in the means for creating an opening in the etch resist material, assuring that the CD produced by the lithography tools is within design specification. Claim 15

provides for assuring that the CD is within design specification using the feedback mechanism that communicates with the means for creating an opening through a layer of etch resist material to control the critical dimension and independent claim 16 provides the feedback mechanism communicating with the lithography tool to control the critical dimension of the opening (that extends through a layer of etch resist material).

Sahin does not anticipate the claims because Sahin fails to provide the claimed feature of *controlling* the critical dimension measurement by *using a feedback mechanism to communicate* with the *means for creating an opening* through a layer of etch resist material, the *means for creating an opening through a layer of etch resist material* being, collectively, *the lithography tools*.

The ANSWER states, on page 10: "In response to Appellants' contention that Sahin does not teach or suggest the claimed feature of controlling the critical dimension measurement by communicating with the means for creating an opening through a layer of etch resist material, Respondent respectfully disagrees." The ANSWER then continues, on page 11, to state that "the module controller 114 may reject the wafer as being out of design specification and direct the inventive system 100 to rework the wafer (see page 16, paragraphs [0210]-[0212] and FIG. 8A(1))."

Appellants respectfully submit that there is a difference between a] assuring that only samples with critical dimensions within design specification are passed on to an etching process and b] *controlling* the critical dimension by *communicating* with the *means for creating an opening* through a layer of etch resist material, i.e., (collectively) "*the lithography tools*", using a feedback mechanism. Sahin does not provide the feature of communicating with the lithography tools and Sahin cannot and does not provide the feature of communicating with the lithography tools to control the critical dimensions.

Sahin merely screens all wafers, sends the acceptable wafers on for further processing, and reworks the wafers that are out of design specification. Sahin may

control which wafers are sent on for etching, but Sahin does not control the critical dimensions, much less by communicating with the lithography tool.

Sahin, as shown in FIGS. 8A(1) and 8A(2), does nothing to assure "that the obtained critical dimension measurement of the features 'openings' created through the patterned masking layer (layer of etch resist material) is within design specification", as alleged in the ANSWER on p. 12, lines 8-11. Rather, Sahin merely assures that the wafers sent on for further processing in the etch operation [812 of FIG. 8A(2)] are those wafers that have critical dimensions that are within design specification. If they are not within design specification, as shown in FIG. 8A(1), they are rejected at step 811 and reworked at step 807 of FIG. 8A(1).

Sahin does NOT provide a feedback mechanism communicating with the means (lithography tool) for creating the features through the patterned masking layer to control the critical dimension measurement of the features by implementing corrections in the means for creating the features through the patterned masking layer. In fact, Sahin provides no feedback mechanism that communicates with the lithography tools at all. FIG. 8A(1) shows that the rejected wafers are reworked at step 807 and Sahin provides no teaching or suggestion that anything is changed in the patterning process that takes place at step 807. Paragraph [0211] of Sahin simply states ". . . to rework the wafer (step 807) as previously described" and the previous description appears in paragraph [0209] which provides ". . . the module controller 114 may direct the inventive system 100 to rework the wafer if possible (step 807) . . . the wafer then may be reprocessed via a lithography tool (not shown)."

There is no control of CD's by communicating with the lithography tool because there is no communication with the lithography tool. There is no feedback mechanism that communicates with the lithography tool and therefore no feedback mechanism that communicates with the lithography tool to control critical dimensions. Appellants again point out the significance of the system overview schematic shown in FIGS. 1A and 1B of Sahin, which show the module controller 114 and the fab controller 116 in apparent communication with a multitude of tools, i.e., etch tool 102, cleaning tool 104, oxidation

tool 106, deposition tool 108, and planarization tool 110, **with the conspicuous absence of a lithography tool**. The module (114) and fab (116) controllers do not communicate with the lithography tools.

Sahin clearly does not disclose communication, much less via a feedback mechanism, with the lithography tool. Therefore, Sahin also does not disclose control of the CD's by communication with the lithography tool, as in the claimed invention.

Applicants respectfully submit that the absence of such disclosure from Sahin is, in effect, conceded in the ANSWER, which states, on page 13, lines 4-8:

> It is further respectfully submitted that to rework the processed wafer mean to improve the processed wafer to obtain the features (openings) that created through the patterned masking layer (layer of etch resist material) that meets the design specification requirements by implementing corrections in the means for creating the features (photolithographic tool).

Applicants respectfully disagree that reworking wafers means implementing corrections in the photolithographic tools. Rather, it is commonly known in the semiconductor manufacturing industry that to "rework" a wafer simply means to process the wafer through the same process again. Generally speaking, there is *no* suggestion that to simply *rework* a wafer means to make any adjustments in the processing of that wafer a second time. Furthermore, according to the common vernacular of those of skill in the semiconductor manufacturing industry, to rework a wafer through a photolithographic operation does NOT mean making any adjustments in the photolithographic process. It merely means, as stated in Sahin, removing the photoresist material, recoating the wafer, then processing the wafer through the photolithographic operation again. Again, Sahin screens all wafers, sends on the wafers that are within design specification, and reworks those wafers that are out-of-spec. If Sahin screens a significant number of wafers and the overwhelming majority of these wafers have critical dimensions within design specifications, with only a minority of the measured wafers falling outside of the design specification limits, there would be **no** motivation to make any adjustments to the lithographic operation and

therefore, as is conventional in the semiconductor manufacturing industry, Sahin would simply rework the wafers without making any adjustments, without controlling the critical dimensions. As such, it is neither conventional nor inherent to implement such corrections when simply reworking wafers.

Sahin clearly does not disclose communicating with the photolithography tools to control CD's by implementing corrections and since it is neither inherent nor conventional to implement corrections in the photolithography tools when simply reworking out-of-spec CD's, Sahin doesn't teach and fails to provide enablement for this feature of *controlling the critical dimension by communicating with the means for creating an opening through a layer of etch resist material, i.e., the lithography tools,* as required in Forrest Laboratories, supra.

In conclusion, reversal of the final rejection of claims 8-11 and 15-17 is requested because these claims are not anticipated by Sahin under 35 U.S.C. § 102(e).